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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,365	11/12/2003	Johannes Becker	BECKER 1	6816

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EXAMINER	
DEBNATH, SUMAN	
ART UNIT	**PAPER NUMBER**
2135	

NOTIFICATION DATE	DELIVERY MODE
08/23/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hittgaines.com

Office Action Summary	Application No.	Applicant(s)	
	10/706,365	BECKER, JOHANNES	
	Examiner	Art Unit	
	Suman Debnath	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in this application.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office Action.

Claim Rejections - 35 USC § 103

3. Claims 1, 2, 4, 5, 8, 9, 11, 12, 15, 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warren (Patent Number: US 6,381,721 B1) in view of Shinmori (Patent Number: US 7,058,856 B2).

4. As to claim 1, Warren discloses an integrated circuit (IC) having a testing port (FIG. 1, column 3, lines 42-50), a system for securing said IC as against subsequent reprogramming (abstract), comprising: port inhibit circuitry located on said IC (FIG. 3, column 8, lines 20-50, "...a receive signal inhibitor 408 which inhibits the receive buffer from allowing any further incoming data..."); and port access circuitry, coupled to said testing port that enables said testing port based on said configuration (FIG. 1, column 3, lines 42-50, "test access port controller" column 11, lines 53-64 and column 9, lines 33-47).

Warren doesn't explicitly disclose inhibit circuitry that modifiable to achieve a configuration that determines an extent to which the testing port is enabled. However, Shinmori discloses inhibit circuitry that modifiable to achieve a configuration that

determines an extent to which the testing port is enabled (column 3, lines 15-25 and lines 40-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren by modifying inhibit circuitry to achieve a configuration that determines an extent to which the testing port is enabled as taught by Shinmori in order to prevent the programmed the contents being read out by a third party.

5. As to claim 8, Warren discloses an integrated circuit (IC) having a testing port (FIG. 1, column 3, lines 42-50), a method of securing said IC as against subsequent reprogramming (abstract), comprising: port inhibit circuitry located on said IC (FIG. 3, column 8, lines 20-50); and enabling said testing port based on the configuration (column 11, lines 53-64 and column 9, lines 33-47).

Warren doesn't explicitly disclose modifying port inhibit circuitry to achieve a configuration that determines an extent to which said testing port is enabled. However Shinmori discloses modifying port inhibit circuitry to achieve a configuration that determines an extent to which said testing port is enabled (column 3, lines 15-25 and lines 40-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren by modifying port inhibit circuitry to achieve a configuration that determines an extent to which said testing

port is enabled as taught by Shinmori in order to prevent the programmed contents from being read out by a third party.

6. As to claim 15, an electronic device, comprising: an integrated circuit (IC) (abstract), including: a testing port (FIG. 1, column 3, lines 42-50), port inhibit circuitry located on said IC (FIG. 3, column 8, lines 20-50), and port access circuitry (FIG. 1, column 3, lines 42-50), coupled to said testing port (FIG. 1), that enables said testing port based on said configuration (column 11, lines 53-64 and column 9, lines 33-47).

Warren doesn't explicitly disclose modifiable inhibit circuitry to achieve a configuration that determines an extent to which said testing port is enabled. However, Shinmori discloses modifiable inhibit circuitry to achieve a configuration that determines an extent to which said testing port is enabled (column 3, lines 15-25 and lines 40-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren by modifiable inhibit circuitry to achieve a configuration that determines an extent to which said testing port is enabled as taught by Shinmori in order to prevent the programmed contents from being read out by a third party.

7. As to claims 2, 9 and 16, Warren doesn't explicitly disclose that the testing port is a Joint Test Action Group (JTAG) port. However, Shinmori discloses that the testing port is a Joint Test Action Group (JTAG) port (column 1, lines 42-48).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren by including testing port as a Joint Test Action Group (JTAG) port as taught by Shinmori in order to make the product as global industry standard by participating in the development of IEEE-SA.

8. As to claims 4, 11 and 18, Warren doesn't explicitly disclose wherein said modifying comprises permanently modifying said port inhibit circuitry prior to delivering said IC to a user thereof. However, Shinmori discloses wherein said modifying comprises permanently modifying said port inhibit circuitry prior to delivering said IC to a user thereof (column 3, lines 15-25 and lines 40-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren by permanently modifying the port inhibit circuitry prior to delivering the IC as taught by Shinmori in order to prevent the programmed contents from being read out by a third party.

9. As to claims 5, 12 and 19, the extent is selected from the group consisting of: fully enabled, only partially disabled, and completely disabled (column 8, lines 20-50 and lines 32-60).

10. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warren in view of Shinmori and further in view of Bos et al. (Patent No.: US 7,124,340 B1).

11. As to claims 6 and 13, neither Warren nor Shinmori explicitly disclose wherein the testing port comprises a direct loopback between input and output pins thereof. However, Bos discloses wherein the testing port comprises a direct loopback between input and output pins thereof (column 7, lines 60-67 and column 8, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren and Shinmori by including a direct loopback between input and output pins thereof as taught by Bos in order to isolate defects within the circuit by supporting loopback testing.

12. Claims 3, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warren in view of Shinmori and further in view of Parulkar (Patent No.: US 6,769,081 B1).

13. As to claims 3, 10 and 17, Warren discloses inhibit circuitry comprises an inhibit bit (column 8, lines 20-50). Neither Warren nor Shinmori explicitly discloses the inhibit bit in a one-time programmable register. However, Parulkar discloses bits in a one-time programmable register (column 1, lines 60-67 and column 2, lines 1-7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren and Shinmori by including a one-time programmable register in order to "program a fuse to de-activate the faulty half and to reconfigure the memory (Parulkar)"

14. Claims 7, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Warren in view of Shinmori and further in view of Hansford (Patent No.: US 6,522,100 B2).

15. As to claims 7 and 14, neither Warren nor Shinmori explicitly disclose wherein the IC is a baseband chip of a mobile communication device. However, Hansford discloses wherein the IC is a baseband chip of a mobile communication device (column 1, lines 45-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren and Shinmori by including a baseband chip of a mobile communication device as taught by Hansford in order to receive a frequency signal or frequency information.

16. As to claim 20, neither Warren nor Shinmori explicitly disclose the electronic device wherein said electronic device is selected from the group consisting of: a mobile telephone, a PDA, an MDA, an MP3 player, and a set-top box (column 1, lines 45-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren and Shinmori by including a electronic device from the group consisting of: a mobile telephone, a PDA, an MDA, an MP3 player, and a set-top box as taught by Hansford in order to receive a frequency signal or frequency information.

17. Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may be applied as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Response to Arguments

18. Applicant's arguments filed 04 June 2007, have been fully considered but they are not persuasive.

Applicant argues that: "Shinmori has not been cited to cure this deficiency of Warren but to disclose modifiable inhibit circuitry to achieve a configuration that determines an extent to which a testing port is enabled. ...Additionally, the Applicant does not find where Shinmori cures the above noted deficiency of Warren. As such, the cited combination of Warren and Shinmori does not establish a prima facie case of obviousness for independent Claims 1, 8, and 15 and Claims that depend thereon."

Examiner has carefully reviewed Applicant's argument and maintains that:

Shinmori discloses inhibit circuitry that modifiable to achieve a configuration that determines an extent to which the testing port is enabled (Shinmori teaches a JTAG

control circuit which can be configured or modified to allow (i.e., enable) or prohibit (i.e., disable) communication of signals is installed between the JTAG port (i.e. testing port) and the TAPs and is controlled by the security bit of the flash ROM. e.g., see col. 3, lines 4-10). Furthermore, Shinmori discloses "a programmer debugs and develops a program by using the JTAG port. When the development ends, he writes "1" in the security but of the flash ROM to input the JTAG control circuit as a prohibit signal and the communication of signals is to be prohibited (Col. 3, lines 8-20)." JTAG port (i.e. testing port) had to be enabled in order for a programmer to debug and develop a program by using the JTAG port. Furthermore, enabling or disabling JTAG port depends upon security bit "1" to input the JTAG control circuit. One of the ordinary skill in the art would understand if security bit "1" prohibit communication to JTAG port (i.e. disables testing port) than JTAG port would be enabled if security bit was not changed to "1" (i.e. remains to "0") (Col. 3, lines 8-20).

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Warren discloses port inhibit circuitry located on integrated circuit (FIG. 3, Col. 8, lines 20-50, "...a receive signal inhibitor 408 which inhibits the receive buffer from allowing any further incoming data...") and port access circuitry coupled to testing port (FIG. 1, Col. 3, lines 42-50, "test access port controller"). Shinmori discloses inhibit circuitry that modifiable to achieve a configuration that determines an extent to which the testing port is enabled (col. 3, lines 4-26 and lines 45-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the teaching of Warren by modifying inhibit circuitry to achieve a configuration that determines an extent to which the testing port is enabled as taught by Shinmori in order to prevent the programmed the contents being read out by a third party.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suman Debnath whose telephone number is 571 270 1256. The examiner can normally be reached on 8 am to 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on 571 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SD

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